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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/608,870	BOHR ET AL.
	Examiner	Art Unit
	Long K. Tran	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1 - 8,10 - 27 is/are pending in the application.

4a) Of the above claim(s) 17 - 24 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1 - 8, 10 - 16, 25, 26 is/are rejected.

7)☒ Claim(s) 27 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to Amendment filed on February 4, 2005.

2. Claim **9** has been cancelled.

3. Claims **1** and **14** have been amended.

4. Claims **25 – 27** have been added.

5. Claims **1 – 8, 10 – 16** and **25 – 27** are presented for examination.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims **1, 2, 8, 10, 11** and **25** are rejected under 35 U.S.C. 102(e) as being anticipated by Chau et al. (US Patent no. 6,653,700).

9. Regarding claim **1**, Chau discloses a apparatus comprising:

a substrate 302 (fig. 3G; col. 4, lines 53, 54 and 55);

a device including a gate electrode 316 (fig. 3G; col. 5, lines 45 and 46) on a surface of the substrate and a first junction and the second junction 321 (fig. 3G; col. 7,

lines 50 – 53; note: substrate surface 303 (labeled by the examiner) identical to 203 (fig. 2); col. 3, lines 45 – 47) in the substrate adjacent to the gate electrode 316 (fig. 3G; col. 5, lines 46 and 46); and

an epitaxial layer 320 (fig. 3G; col. 6, lines 45 – 47) comprising silicon alloy disposed in each of the first junction and second junction such that a surface of the first junction region 330 (fig. 3G) and a surface of the second junction region 330 (fig. 3G) are in non-planar relationship with surface 303 of the substrate.

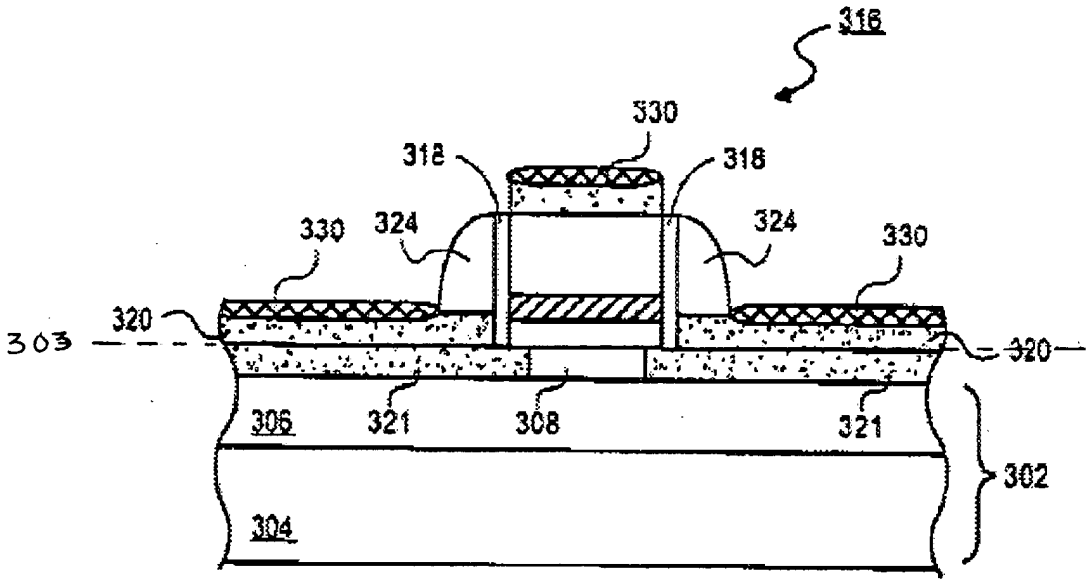

FIG. 3G

Regarding claim **2**, Chau discloses a surface 303 (fig. 3G) of the substrate defines a top surface of the substrate and the surface of the first junction region 330 (fig. 3G) and the surface of the second junction region 330 (fig. 3G) are superior to the top surface of the substrate (fig. 3G).

Regarding claim **8**, Chau discloses a surface of the substrate proximate to the first junction region defines a first substrate sidewall surface and a surface of the substrate proximate to the second junction region defines a second substrate sidewall surface 318 (fig. 3G) and the silicon alloy material 320 (fig. 3G) disposed in the first junction region is attached to the first substrate sidewall surface and the silicon alloy material disposed in the second junction region is attached to the second substrate sidewall surface 318 (fig. 3G).

Regarding claim **10**, Chau discloses the silicon alloy material comprises silicon germanium (col. 6, lines 46 and 47).

Regarding claim **11**, Chau discloses a layer 330 (fig. 3G; col. 8, lines 53 and 62) of silicide material on the surface of the first junction region, the surface of the second junction region, and the gate electrode, wherein the layer of silicide material comprises titanium silicide (col. 8, line 62).

Regarding claim **25**, Chau discloses an apparatus comprising:

a substrate 302 (fig. 3G; col. 4, lines 53, 54 and 55);

a device including a gate electrode 316 (fig. 3G; col. 5, lines 45 and 46) on a surface of the substrate and a first junction and the second junction 321 (fig. 3G; col. 7, lines 50 – 53; note: substrate surface 303 (labeled by the examiner) identical to 203 (fig. 2); col. 3, lines 45 – 47) in the substrate adjacent to the gate electrode 316 (fig. 3G; col. 5, lines 46 and 46); and

an epitaxial layer 320 (fig. 3G; col. 6, lines 45 – 47) comprising silicon alloy disposed in each of the first junction and second junction such that a surface of the first

junction region 330 (fig. 3G) and a surface of the second junction region 330 (fig. 3G) are in non-planar relationship with surface 303 of the substrate. Wherein the silicon alloy material has one of the same crystallographic characteristic, a same crystal structure, and a same crystal grade as the substrate (note: the substrate in Chau's device is a monocrystalline (col. 4, lines 49+) similar to the claimed substrate; the silicon alloy in Chau's device is a single crystalline silicon (epitaxial silicon) (col. 7, lines 9 – 15) similar to the claimed silicon alloy layer, therefore, the silicon alloy material in Chau's device has one of the same crystallographic characteristic, a same crystal structure, and a same crystal grade as the substrate).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims **3, 4, 5, 6, 7, 14, 15, 16** and **26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (US Patent no. 6,653,700).

Regarding claim **3**, Chau discloses the claimed invention of claim 1 and shows the surfaces of the first junction region and the second junction region are superior to the top surface of the substrate by length in the range of between 50 nanometers and 100 nanometers (col. 7, line 29) but not in the range of between 5 – 49 nanometers and 101 – 150 nanometers as claimed in the present claim 3.

However, it would have been well known in the art that the selection of those parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, or in conbination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Moreover, the height of the junction regions has not been alleged by applicant to be of significant importance for patentability.

Regarding claim **4**, Chau discloses the claimed invention of claim 1 and shows the first junction region and the second junction region define a depth in the range of

less than 50 nanometers (same thickness of intrinsic silicon cited in claim 3) but not in the range of between 51 – 250 nanometers as claimed in the present claim 4.

However, it would have been well known in the art that the selection of those parameters such as **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, would have been obvious and involve routine optimization which has been held to be within the level of ordinary skill in the art. "Normally, it is to be expected that a change in **energy, concentration, temperature, time, molar fraction, depth, thickness, etc.**, or in conbination of the parameters would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).*

Moreover, the depth has not been alleged by applicant to be of significant importance for patentability.

Regarding claims **5, 6** and **7**, Noguchi et al. disclose claimed invention of claim 1, except for the substrate is under a strain caused by a silicon alloy lattice spacing of the silicon alloy (cited in claim 5); the silicon alloy material has a silicon alloy lattice spacing that is different than a lattice spacing of the substrate material (cited in claim 6); and the substrate is under a strain caused by a silicon alloy lattice spacing being a larger lattice spacing than the lattice spacing of the substrate material.

However, Noguchi et al. show the device structure similar to the claimed structure. Therefore, it is fair to say that, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to recognize Noguchi's device would have a substrate being under a strain caused by a silicon alloy lattice spacing of the silicon alloy; the silicon alloy material has a silicon alloy lattice spacing that is different than a lattice spacing of the substrate material; and the substrate is under a strain caused by a silicon alloy lattice spacing being a larger lattice spacing than the lattice spacing of the substrate material.

Regarding claim **14**, Chau discloses an apparatus comprising:

a substrate 302 (fig. 3G; col. 4, lines 53, 54 and 55);

a device including a gate electrode 316 (fig. 3G; col. 5, lines 45 and 46) on top surface of the substrate and a first junction and the second junction 321 (fig. 3G; col. 7, lines 50 – 53; note: substrate surface 303 (labeled by the examiner) identical to 203 (fig. 2); col. 3, lines 45 – 47) in the substrate adjacent to the gate electrode 316 (fig. 3G; col. 5, lines 46 and 46); and

a silicon alloy material layer 320 (fig. 3G; col. 6, lines 45 – 47) disposed in each of the first junction and second junction such that a surface of the first junction region 330 (fig. 3G) and a surface of the second junction region 330 (fig. 3G) are superior to the top of the surface 303 of the substrate by a length sa discussed in claim 3 above.

Chau does not explicitly expresses the silicon alloy lattice spacing being different than the lattice spacing of the substrate disposed in each of the first junction region and the second junction region and the length sufficient to cause a strain in the substrate.

However, Chau show the device structure similar to the claimed structure including similar materials. Therefore, it is fair to say that, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to recognize Chau's device would have a silicon alloy material having a silicon alloy lattice spacing that is different than a lattice spacing of the substrate; and since the length of Chau's device is almost equal to the length of the claimed invention, Chau's device would have length sufficient to cause a strain in the substrate as claimed.

Regarding claim **15**, Chau discloses the substrate comprises an N-type channel/well of silicon (col. 6, lines 28 and 39 – 41; note: for a PMOS device the channel is an N-type) having an electrically negative charge, and the silicon alloy material comprises a P-type junction region material having an electrically positive charge.

Regarding claim **16**, Chau discloses the silicon alloy is silicon germanium that would have a lattice spacing larger than a lattice spacing of N-type silicon channel/well and the strain would be a compressive strain.

Regarding claim **26**, Chau discloses the claimed invention of claim 25 but does not explicitly expresses the silicon alloy lattice spacing being different than the lattice spacing of the substrate disposed in each of the first junction region and the second junction region and the length sufficient to cause a strain in the substrate.

However, Chau show the device structure similar to the claimed structure including similar materials. Therefore, it is fair to say that, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to recognize Chau's device would have a silicon alloy material having a silicon alloy lattice spacing that is different than a lattice spacing of the substrate; and since the length of Chau's device is almost equal to the length of the claimed invention, Chau's device would have length sufficient to cause a strain in the substrate as claimed.

12. Claims **12** and **13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (US Patent no. 6,653,700) in view of in view of Kim et al. (US Patent Application Publication No. 2003/0186508).

13. Regarding claim **12**, Chau discloses the claimed invention of claim1 and 11 except for a layer of conformal etch stop material on the layer of silicide material, wherein the layer of etch stop material comprises silicon dioxide, phosphosilicate glass, silicon nitride, and silicon carbide.

However, Kim shows an etch stop layer 140 (fig. 13; [0039]) formed of silicon nitride on a silicide layers 137a and 137b (fig. 13; [0035]).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide a silicon nitride etch stop layer as taught by Kim over the silicide layer 330 of Chau's device, in order to protect the transistor during forming contact hole process ([0040]).

Regarding claim **13**, Kim discloses an ILD 145 formed of PSG ([0039]).

Allowable Subject Matter

14. Claim **27** is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. The following is an examiner's statement of reasons for the indication of allowable subject matter: Claim **27** is allowable over the prior art of record because none of the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach:

The silicon alloy material 470, 480 (figs. 3 – 7) extends below the surface of the substrate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

16. Applicant's arguments with respect to claims 1 – 16 have been considered but are moot in view of the new ground(s) of rejection.

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Tran LT

March 29, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800